Effect of Lead Wire Lengths on Protector Clamping Voltages

By O. Melville Clark and Joseph J. Pizzicaroli

Originally presented at the Federal Aviation Administration - Florida Institute of Technology Workshop on Grounding and Lightning Technology: March, 1979 - Melbourne, Florida

Abstract

Under high current pulse conditions, excessive lead lengths on suppressor components can be responsible for destruction of the protected circuit. This is caused by voltage build-up across the small but finite amount of inductance in the interconnecting leads of the protector. Some suppressor devices have been tested and observed to have more than twice the specified clamping voltage which was subsequently shown to be caused by inductive effects. Problems and corrective measures are illustrated and discussed in this paper.

SEMICONDUCTOR FAILURE THRESHOLDS

MOS and small area geometry semiconductors are particularly vulnerable to the effects of transient voltages. Unfortunately there has been very little information published on this subject. The work reported by Van Keuren [1] illustrates how fragile CMOS and TTL devices can be. Minimum failure pulse voltage thresholds are shown in Table 1.

TABLE 1 - MINIMUM FAILURE THRESHOLDS OF CMOS AND TTL

DEVICE TYPE	PULSE WIDTH					
	20 µs	2 µs	1 µs	0.02 µs	0.01 µs	0.025 µs
55107	22 V	16 V		22 V		
55109	36 V	38 V		60 V		
5404			30 V		50 V	120 V
54L30			20 V		50 V	90 V

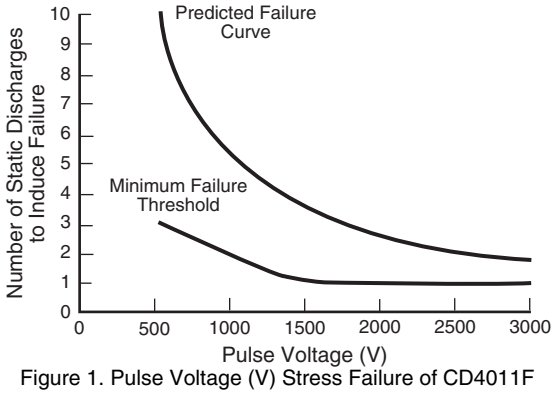


Figure 1. Pulse Voltage (V) Stress Failure of CD4011F

Electrostatic Discharge (ESD) failures of MOS microcircuits have been measured by Gallace and Pujol [2]. Comparisons among several suppliers indicate that failure levels can be a function of manufacturing technique. Repeated step stressing of a sample of 25 CD4011AF type devices shows that at a given stress level devices would eventually fail, as shown in Figure 1.

EQUIVALENT CIRCUIT OF PROTECTOR

The equivalent circuit of a silicon transient suppressor, such as the Transient Voltage Suppressor, is shown in Figure 2. All parameter values are fixed by manufacturing processes and device construction except L_1, the inductance resulting from the lead wires connecting the protector across the circuit for which protection is intended. Normal wiring practice results in lead lengths of the order of centimeters. In some power installations this has been observed to be of the order of feet.

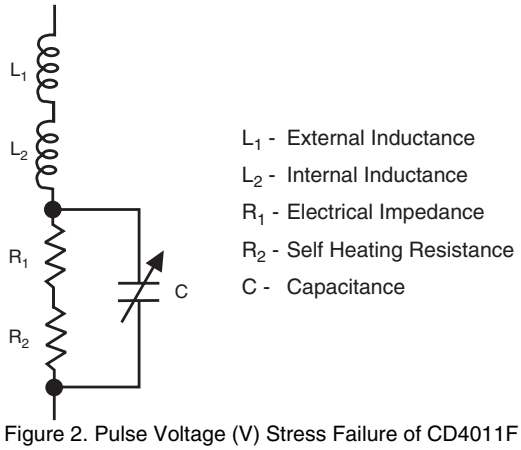


Figure 2. Pulse Voltage (V) Stress Failure of CD4011F

The inductance within an axial leaded part, as represented by L_2, is of the order of 10^{-8} H while the inductance within a modular assembly can be one to two orders of magnitude greater, depending on the design and the number of subcomponents. The capacitance of a silicon avalanche suppressor can vary over an order of magnitude, depending on the degree of reverse biasing.

TRANSIENT VOLTAGE RISE-TIMES

A. EMP: Voltage rise-times of EMP (Electromagnetic Pulse) transients, as generated by high altitude nuclear detonations, are 5 kV/ns. The presence of even a small amount of inductance in the protector circuit can have very profound results on the effectiveness of a protector device. This is illustrated with the oscillographs in Figure 3 and 4.

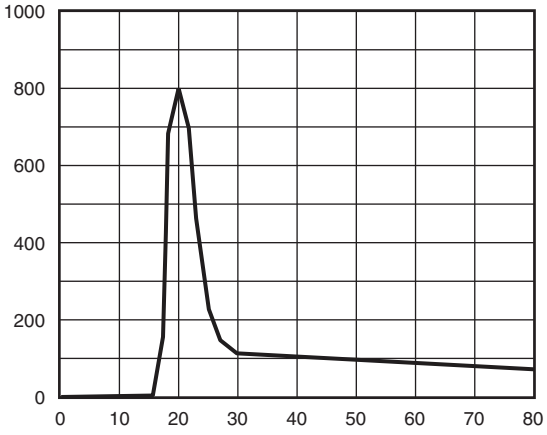


Figure 3. 7.5 cm Lead Wire

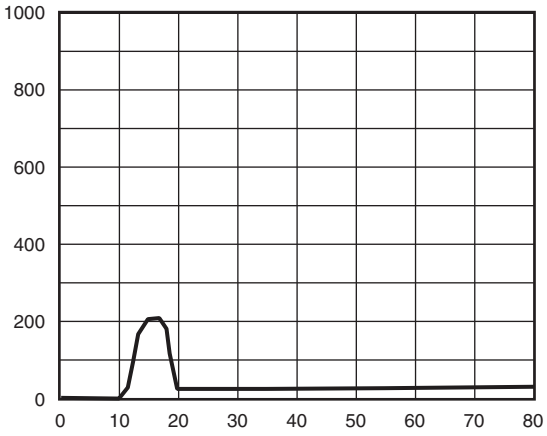


Figure 4. Zero Length Lead Wire

In Figure 3, a 30 V Transient Voltage Suppressor in the DO-13 package was pulsed with a 100 A 4 kV/ns rise-time transient. With 7.5 cm leads on each end, at which current was injected and voltage measured, the overshoot voltage is slightly greater than 800 V. The energy under this curve is calculated to be 70 mJ, sufficient energy to destroy most types of MOS and some TTL devices. By reducing the lead length to zero and repeating the pulsing, the overshoot voltage is reduced to about 200 V. The energy under this curve is less than 1 mJ, below the destruct threshold of MOS and TTL devices.

B. Lightning and Inductive Switching: From measurements made on 120 V_{AC} power systems, Martzloff [3] has proposed a waveform with a frequency of 100 kH. The lightning stroke, which is usually reported with current rise-times ranging from 1 to 3 ms has been more recently measured by Llewellyn [4] to be as low as 500 ns. Transients on shipboard AC power systems have been defined by MIL-STD-1339 as having transient rise-times of 1.5 ms.

Normal wiring practices are usually considered adequate for protection of electronic circuitry. “Normal” and “adequate” are relative terms and usually prevail under conditions in which equipment performance is acceptable. What is normal and adequate protection for vacuum tubes is not the same for power semiconductor devices. Protection for microcircuits is also quite different from power semiconductors. With increased usage of microprocessors and other small area geometry semiconductors, equipment is becoming more vulnerable to transient voltages, under both single pulse and repetitive pulse conditions.

INDUCTIVE EFFECTS IN COMPONENT LEADS

A. Calculation: The inductance in a straight wire appears, at first glance, to be very small and insignificant. Assuming a value of 1 mH/m for a straight wire, most lead wires have inductance values in the nH region. The voltage drop developed across an inductor under pulse conditions is expressed as:

$$V_{(t)} = L\frac{dI}{dt}$$

where L is inductance in henrys

$\frac{dI}{dt}$ is the rate change of current

For the fast rise-times of EMP as shown above, the associated problems are obvious; however, for the slower rise-time of switching and induced lightning the degree of exposure and protection required can be defined only after carefully studying all boundary conditions.

B. Case Study: In the following application, a silicon transient suppressor is being used to both regulate the voltage to power a telecommunications repeater and also provide transient suppression. The schematic is shown in Figure 5. This is one of two repeaters powered and protected by the same component.

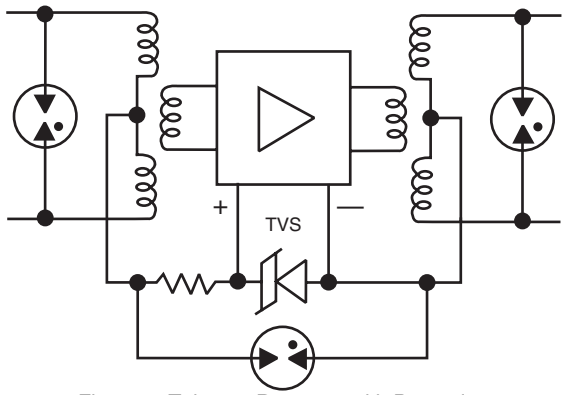


Figure 5. Telecom Repeater with Protection

The microcircuitry used in this equipment has some well defined failure levels; 20 V in the positive direction and 6.5 V in the negative direction. The suppressor has a well defined clamping voltage in the avalanche direction under a specified rise-time. The forward polarity measurements are specified at 100 A with an 8.4 ms, 1/2 sine wave pulse. To determine higher current capability, pulse tests were made with a 1.2 x 50 ms waveform.

During the process of taking data, small differences in lead length in the protection circuit were observed to have profound effect on the suppression capability of the device. Measurements extended over the range from 100 A to 500 A with lead lengths from the body of the device of zero, 1.0 cm and 2.0 cm. Tests were made on a molded 1.5 kW Transient Voltage Suppressor. The peak clamping voltage was plotted against pulse current as shown in Figure 6.

After tests were made with 0.0, 1.0 cm and 2.0 cm lead lengths, the plastic body was carefully cut away leaving only the cell containing the junction and the leads. Voltage measurements were then made across the cell, virtually eliminating inductance within the package. A lead length of 2 cm has a peak clamping voltage of 4 V at 100 A and 13.5 V at 500 A. By contrast, the cell only has a peak clamping voltage of 1.3 V at 100 A and 3 V at 500 A. Voltage probe placement for taking measurements is shown in Figure 7.

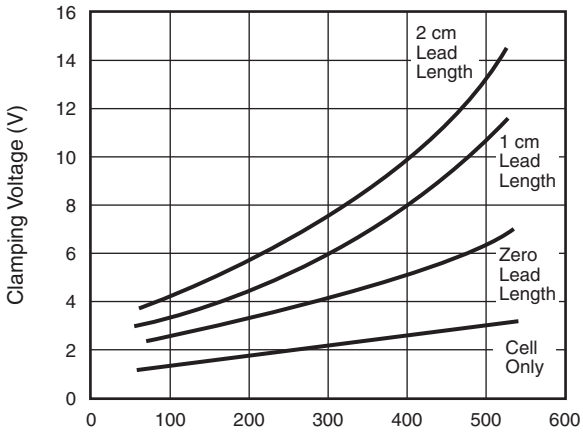
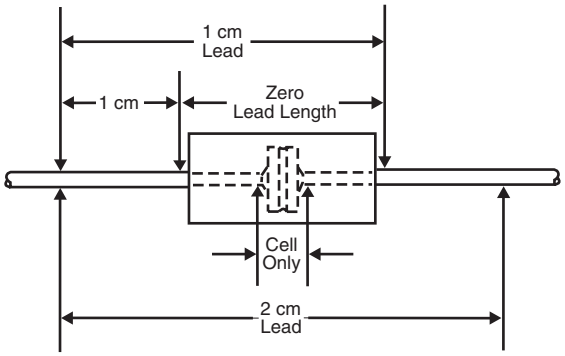


Figure 6. Clamping Voltage vs. Pulse Current



Voltage Probe Placement

Figure 7. Voltage Probe Placement

Voltage drops across the lead wires contributing to peak clamping voltage can be attributed to both resistive and inductive components. Calculations were made for both resistive and inductive voltage drops for a 1.0 cm 0.040" diameter copper wire at pulse current levels from 100 A to 500 A. Rise-time is 1.2 ms. This data is shown in Table 2.

Note that the calculated inductive voltage drop compares favorably with the measured voltage drop while the resistive component contributes less than 10 % of the total.

TABLE 2 - PULSE CURRENT LEVEL AND VOLTAGE DROP			
PULSE CURRENT (A)	MEASURED VOLTAGE DROP (V)	CALCULATED RESISTIVE VOLTAGE DROP (V)	CALCULATED INDUCTIVE VOLTAGE DROP (V)
100	0.75	0.019	0.83
200	1.3	0.038	1.66
350	2.3	0.066	2.91
500	3.3	0.095	4.16

CLAMPING VOLTAGE OF AC PROTECTOR

In power systems, it is quite easy to place a modular assembly protector in a convenient mounting location rather than the most effective one, especially in retrofit applications. These components are sometimes bulky and do not always conveniently fit the desired location. To illustrate reduced effectiveness in an AC power transient suppressor, a module was measured for peak clamping voltage having lead lengths of 24", 48", and 72". Pulse currents were 100 A, 200 A, 300 A and 400 A with a wave form of 1.2 x 50 ms. Lead length vs. additive peak clamping voltage plotted here, is that value above the normal clamping voltage with zero lead length.

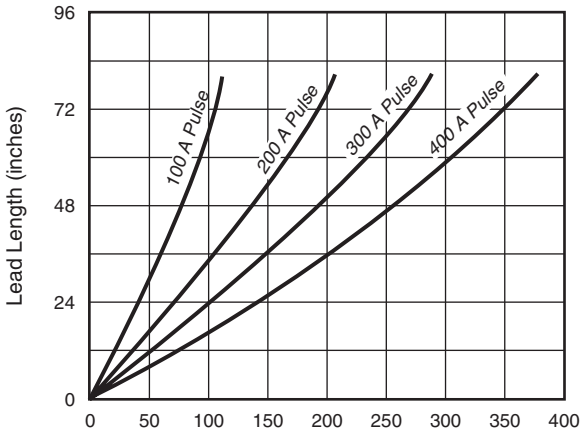


Figure 8. Lead Length vs. Clamping Voltage

Note that the additive clamping voltage can be down in the range of 35 V at 100 A for 24" leads extending up to 350 V at 400 A for 72" leads. An oscillograph depicting optimum protection at 100 A and 400 A is shown in Figure 9. The 100 A pulse is being clamped at about 215 V and 400 A pulse at 265 V. The peak clamping voltage is substantially increased by the inductive effects of 72" leads as shown in Figure 10. In this oscillograph, the 100 A pulse produced a peak of about 320 V and 400 A pulse produced a peak of about 615 V. The inductive overshoot illustrated in Figure 10 is quite profound by comparison with Figure 9.

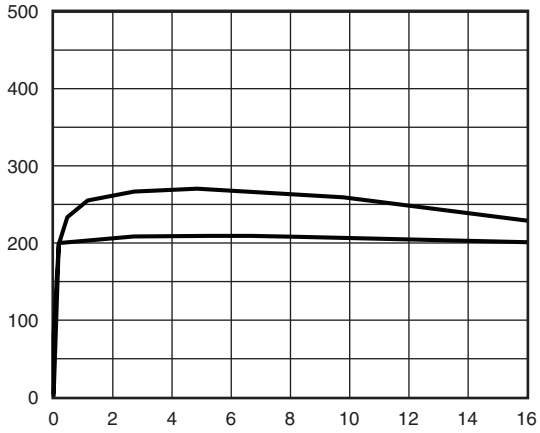


Figure 9. AC Protector, Optimum Protection

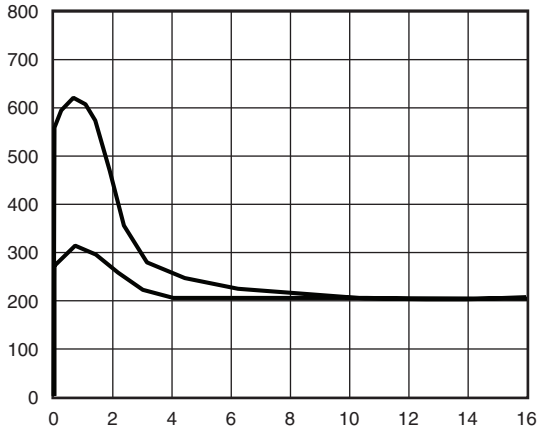


Figure 10. AC Protector, 72" Leads

CLAMPING VOLTAGE OF MICROCIRCUIT PROTECTOR

An ICT-5 type Transient Voltage Suppressor, designed for protecting low voltage logic circuits, was pulsed at levels of 100 A, 200 A, 300 A, 400 A and 500 A with a 1.2 x 50 ms waveform. Voltage drop was measured across the leads at distances of 0.0, 1.0 cm and 2.0 cm from the body of the package, adding a total of 4.0 cm 0.030 diameter straight wire contributing to inductance and subsequently adding to the peak clamping voltage. A graph plotting total lead length vs. peak clamping voltage is shown in Figure 11. These curves are plotted as additive above the breakdown voltage

(BV) at 1 mA, which was 6.3 V for the device tested. The clamping voltages increase with pulse current using zero lead length due both to the electrical impedance and thermal self-heating effect on the silicon pn junction. Observe that the clamping voltage covers a very broad range, from 3.6 V above BV to 24 V above BV depending on peak current and insertion method.

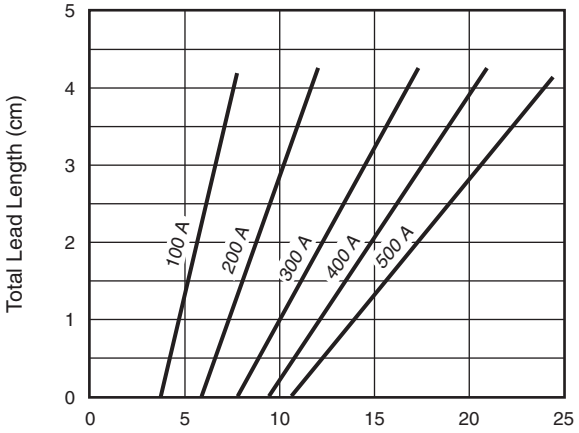


Figure 11. Lead Length vs. Peak Clamping Voltage

REDUCING INDUCTIVE EFFECTS

The most obvious method of reducing inductive effects and thus optimizing protector capability is to reduce lead wire lengths in the protector circuit. If it is not possible to reduce the conductor length, other options are available. Inductance in a given length of conductor can be reduced by replacing a small diameter wire with a wide strip conductor. On circuit boards, a ground plane on one or both sides of the board has been used by the author as a method for optimizing protector clamping.

Since voltage drop across the lead length is a function of the transient rise-time, it may be feasible to add series inductance between the transient source and the protector to reduce the risetime and subsequently the peak clamping voltage. A Transient Voltage Suppressor used for 5 V logic protection was tested with a 300 A pulse having a 1.2 x 50 ms waveform with voltage measurements made at 2.0 cm from each end of the body of the device. This is shown in Figure 12, peaking at 24 V. Placing a 12 mH choke ahead of the suppressor to reduce the rise-time, reduced the peak to 19 V and using 24 mH reduced the peak to 17 V. These curves are also shown in Figure 12.

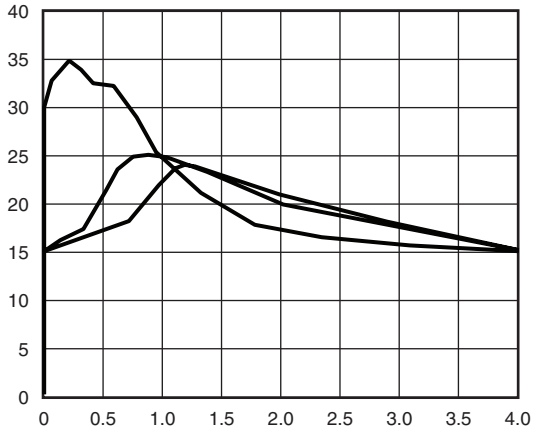


Figure 12. AC Protector, 72" Leads

CONCLUSION

Inductive effects can be, and often are, a source of abnormally high peak clamping voltages compared to the inherent capability of a Transient Voltage Suppressor. These high clamping voltages can cause failure of vulnerable electronic components; thus a suppressor capable of providing adequate protection can be rendered useless due to poor insertion methods. So it behooves the design engineers working on both mechanical layout and circuit design to be acutely aware of inductive effects and the problems which they can cause along with corrective measures in order to optimize transient voltage protector components.

References:

1. E. Van Keuren, “Effects of EMP Induced Transients on Integrated Circuits”, IEEE Electromagnetic Compatibility Symposium Record, October, 1975.
2. L. Gallace & H.J. Pujol, “The Evaluation of CMOS Static-Charge Protection Networks and Failure Mechanisms Associated With Overstress Conditions as Related to Device Life”, presented at the 1977 Reliability Physics Symposium. April, 1977.
3. F.D. Martzloff, “A Guidance on Transient Overvoltages in Low Voltage AC Power Circuits”. GE Report No. 77CRCD221, September, 1977.
4. Sigrid K. Llewellyn, “Broadband Magnetic Field Waveforms Radiated from Lightning”. Masters Thesis, Florida Institute of Technology, 1977.